

Tool helps you floorplan chips

THE IC WIZARD FLOORPLAN-SYNTHESIS TOOL from Aristo Technology lets you create and optimize alternative floorplans for block-level (core-

based) chip designs. You can use the tool at multiple design points—from architectural planning, to checking physical-interconnect feasibility, down through physical implementation. IC Wizard's floorplans are physically and timing-correct and minimize routing congestion, aiding placement-and-routing convergence.

Block-level floorplan exploration lets you evaluate floorplans based on timing, area, interconnect length, or other user-defined parameters. When you use the tool during RTL design, IC Wizard helps you choose the floorplan that best meets your design criteria for size, power, and speed. You then rerun IC Wizard at the gate-level and again after physical implementation, updating the floorplan with more accurate data as it becomes available.

Block descriptions to IC Wizard can be soft, hard, and firm cores. Inputs to the tool include design descriptions, block libraries, process data,

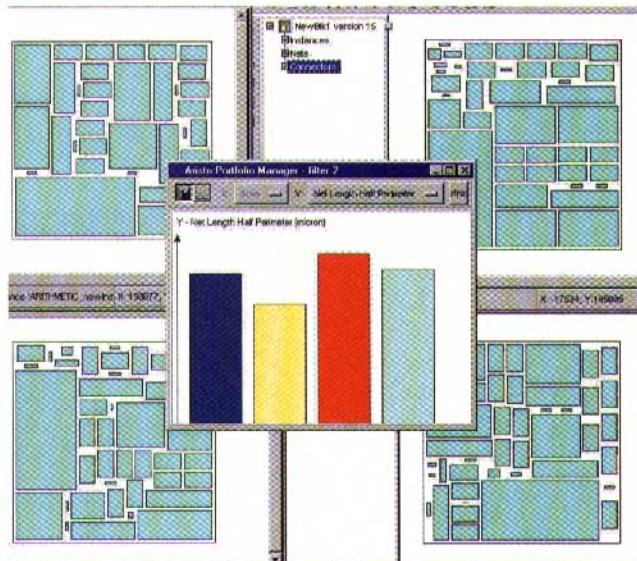
and user constraints. Netlist and soft-block input may be in Verilog or VHDL; hard-block input is in GDS II. Depending on where in the design flow you use the tool, IC Wizard optimizes the floorplans it generates based on

your design constraints, along with synthesis, module compilation, and place-and-route results. Along with floorplan alternatives, the tool also produces the design's global routing. IC Wizard runs on Windows NT and Unix platforms, and prices start at \$100,000.

—by Jim Lipman

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Along with generating floorplan alternatives for block-based chip designs, IC Wizard lets you compare the alternatives based on timing, area, and interconnect-length criteria.